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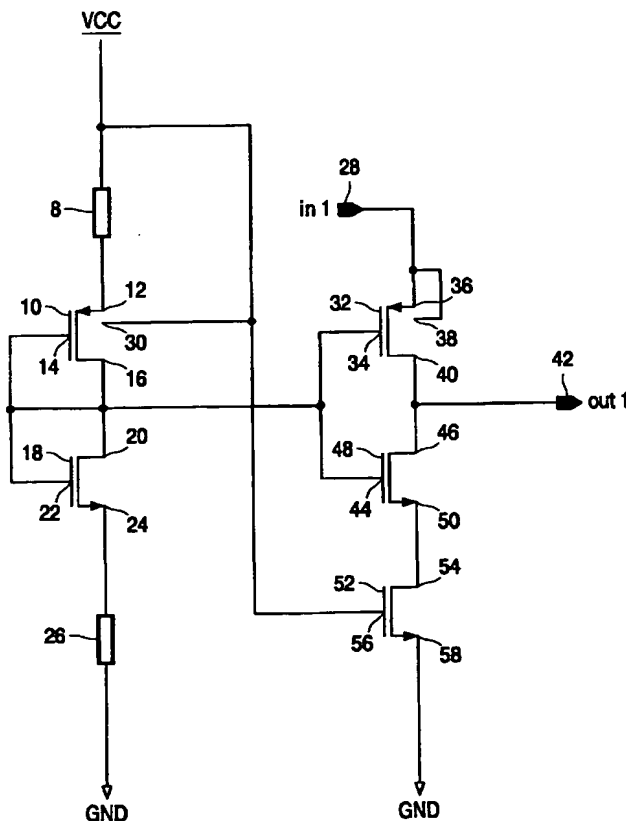
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(54) Title: FAIL-SAFE METHOD AND CIRCUIT



(57) Abstract: A method and a circuit for producing a fail-safe output signal in case of an open circuit condition of an input pad of a digital circuit unit, comprising a first inverter stage (10, 18) providing a constant switch level; a second inverter stage (32, 44) providing a variable switch level that depends of the signal level of the input pad (28) and comparing the constant switch level of the first inverter stage (10, 18) with the variable switch level of the second stage (32, 44) and providing an output signal at an output terminal (42) thereof if the variable switch level of the second stage (32, 44) is greater than the constant switch level; and an additional circuit element (52) connected in series with the second inverter (32, 44) for decreasing the switch level of the second inverter stage (32, 44).



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Minimum documentation searched (classification system followed by classification symbols)

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Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 288 577 B1 (WONG ANTHONY YAP) 11 September 2001 (2001-09-11) cited in the application column 1, line 23 - column 2, line 22; figure 1 column 3, line 30 - column 4, line 59; figure 4	1, 2, 11
A	US 6 320 406 B1 (CARVAJAL FERNANDO D ET AL) 20 November 2001 (2001-11-20) cited in the application the whole document	1, 2, 11



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Patent family members are listed in annex.

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 0174, no. 01 (E-1404), 27 July 1993 (1993-07-27) & JP 5 075430 A (MITSUBISHI ELECTRIC CORP), 26 March 1993 (1993-03-26) abstract	1,2,11
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US 4709172	A	24-11-1987	NONE	

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